CMOS Ultralow Power Brain Signal Acquisition Front-Ends: Design and Human Testing

Alireza Karimi-Bidhendi, *Student Member, IEEE*, Omid Malekzadeh-Arasteh, *Student Member, IEEE*,
Mao-Cheng Lee, *Student Member, IEEE*, Colin M. McCrimmon, *Student Member, IEEE*, Po T. Wang, *Member, IEEE*,
Akshay Mahajan, *Student Member, IEEE*, Charles Yu Liu, Zoran Nenadic, *Senior Member, IEEE*, An H. Do,
and Payam Heydari, *Fellow, IEEE*

***Abstract*—Two brain signal acquisition (BSA) front-ends incorporating two CMOS ultralow power, low-noise amplifier arrays and serializers operating in MOSFET weak inversion region are presented. To boost the amplifier's gain for a given current budget, cross-coupled-pair active load topology is used in the first stages of these two amplifiers. These two BSA front-ends are fabricated in 130 and 180 nm CMOS processes, occupying 5.45 mm^2 and 0.352 mm^2 of die areas, respectively (excluding pad rings). The CMOS 130-nm amplifier array is comprised of 64 elements, where each amplifier element consumes 0.216 μW from 0.4 V supply, has input-referred noise voltage (IRNoise) of 2.19 μV_{RMS} corresponding to a power efficiency factor (PEF) of 11.7, and occupies 0.044 mm^2 of die area. The CMOS 180 nm amplifier array employs 4 elements, where each element consumes 0.69 μW from 0.6 V supply with IRNoise of 2.3 μV_{RMS} (corresponding to a PEF of 31.3) and 0.051 mm^2 of die area. Noninvasive electroencephalographic and invasive electrocorticographic signals were recorded real time directly on able-bodied human subjects, showing feasibility of using these analog front-ends for future fully implantable BSA and brain– computer interface systems.**

***Index Terms*—Analog front-end (AFE), CMOS, electrocorticography (ECoG), electroencephalogram (EEG), instrumentation amplifier (InAmp), noise efficiency factor (NEF), operational transconductance amplifier (OTA), power efficiency factor (PEF), ultra-low power (ULP), weak inversion (WI) region.**

I. INTRODUCTION

IT IS estimated that every year there are ~500,000 new cases of spinal cord injury (SCI) worldwide [1]. This condition substantially decreases independence and quality of life of those affected, and the resulting disability and comorbidities pose a significant economic burden on the individual as well as on society. Since there are no satisfactory means to restore motor function after SCI, novel approaches to address this problem are needed. Bypassing the damaged spinal cord by means of a brain-computer interface (BCI), which enables direct brain control of prostheses, constitutes one such approach. Non-invasive electroencephalogram (EEG)-based BCIs have the capacity to restore basic ambulation after SCI [2], [3], although their applicability is limited by the low information content (i.e., limited bandwidth and low spatial resolution) of EEG signals. Invasive BCIs, on the other hand, have enabled control of multi-degree-of-freedom robotic prostheses [4]. However, they utilize bulky and power-hungry general-purpose recording hardware, and rely on skull-protruding electronic components. Furthermore, these systems typically employ intracortically implanted microelectrode arrays, which can trigger foreign body responses such as inflammation and scarring, ultimately leading to failure of the system within months to few years [5]. These factors represent a serious obstacle to a widespread adoption of invasive BCI technology.

These problems may be addressed by developing a fully implantable BCI system that uses highly stable electrocorticogram (ECoG) signals [6]. Such a BCI system is envisioned to consist of ECoG electrodes, amplifiers, a processor, and a wireless module to control and communicate with output devices (e.g., prostheses), all implemented in a miniaturized form factor and operating in a low-power regime in order to facilitate permanent implantation. Since ECoG electrodes are placed above the arachnoid layer without breaching the neuronal tissue, ECoG signals have long-term stability [6], [7], while providing the spatiotemporal resolution necessary for high-performance BCI applications [8], [9]. In particular, studies have shown that the ECoG high-γ frequency band (70–120 Hz) exhibits spatially localized amplitude modulation that is correlated with individual's physical movements [10], and this feature has been used to decode arm [11] and finger movements [12]. Chronic *in vivo* recording of ECoG signals has been used for neurological treatment. The Medtronic Activa PC+S system [13], [14], was used in patients having Parkinson disease with ECoG electrode strips implanted over the motor cortex and depth electrodes in the subthalamic nucleus [15]. Chronic recordings from these areas

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A. Karimi-Bidhendi, O. Malekzadeh-Arasteh, M.-C. Lee, and P. Heydari are with the Department of Electrical Engineering and Computer Science, University of California, Irvine, CA 92697 USA (e-mail: akarimb@uci.edu; omalekza@uci.edu; maochenl@uci.edu; payam@uci.edu).

C. M. McCrimmon, P. T. Wang, and Z. Nenadic are with the Department of Biomedical Engineering, University of California, Irvine, CA 92697 USA (e-mail: cmccrimm@uci.edu; ptwang@uci.edu; znenadic@uci.edu).

A. Mahajan is with Broadcom, Ltd., San Diego, CA 91127 USA (e-mail: akshaym@uci.edu).

C. Y. Liu is with the Department of Neurosurgery, University of Southern California, Los Angeles, CA 90033 USA (e-mail: chasliu@cheme.caltech.edu).

A. H. Do is with the Department of Neurology, University of California, Irvine, CA 92697 USA (e-mail: and@uci.edu).

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were used to study the association between gamma band oscillations and dyskinesia. The Activa PC+S system was also used for recording signals from ECoG electrode strips over the motor cortex of a patient with amyotrophic lateral sclerosis (ALS) to facilitate BCI-control of a virtual keyboard [16]. Finally, as shown in prior art, a fully implantable system eliminates the need for bulky skull-protruding components, often employed in the state-of-the-art invasive BCIs, as well as bulky recording hardware and external computers.

There has been extensive research on low-power amplifier and amplifier array designs for neural signal sensing applications, which vary substantially in frequency and dynamic range. For example, in [17], the authors present a folded-cascode operational transconductance amplifier (OTA) using current-splitting and current-scaling techniques with a cascaded 6th-order band-pass filter for detecting epileptic fast ripples between 250 and 500 Hz. The stack of 4 transistors and large degeneration resistors in this design increase the required supply voltage to accommodate sufficient output voltage headroom. In [18], a closed-loop neural recording amplifier has been developed that utilizes a T-network in its feedback path in order to achieve high input impedance and common-mode rejection ratio (CMRR) within a small chip area. The authors argued that the T-network in the feedback path is useful when the routing area overhead, crosstalk and input-referred noise (IRNoise) do not dominate the performance [18].

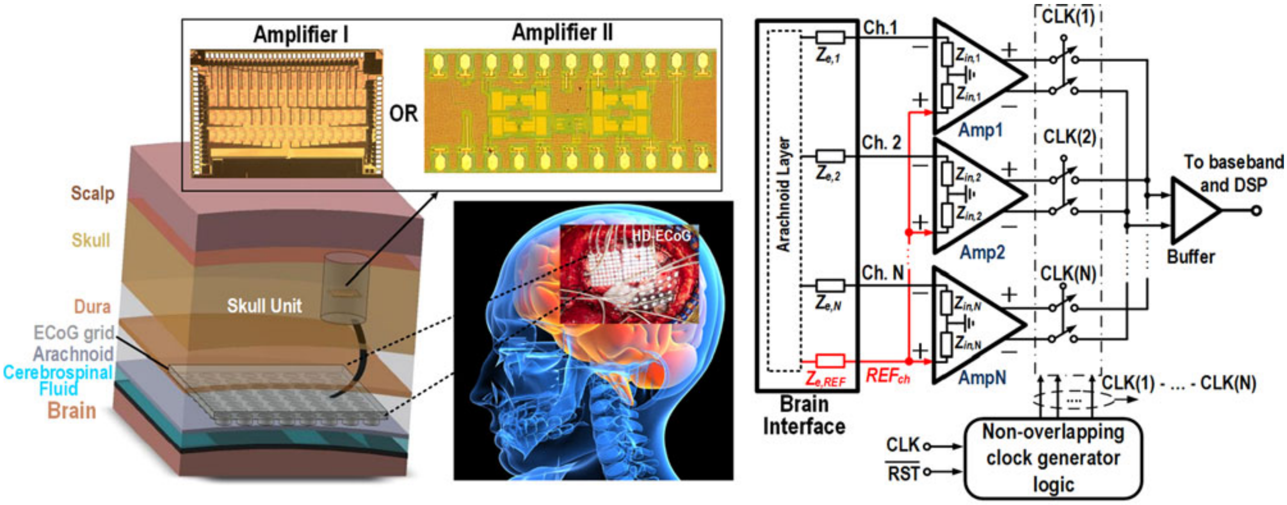
Most of the previously developed neural sensing amplifiers focus on EEG or single-unit recordings. Consequently, their designs are not optimal for use in other recording modalities, such as ECoG. Moreover, a few studies that exist with analog front-end (AFE) designs for ECoG recording lack *in vivo* experimental validation in humans. For example, [19] presents a 32-channel integrated circuit (IC) for ECoG recording, followed by *in vivo* measurements in a rat. The power consumption of this system is too high, making it unsuitable for human ECoG signal acquisition, especially in a fully implantable form. In [20], an ECoG/EEG IC has been introduced which records signals in 4 different sub-bands as opposed to simultaneously capturing the complete ECoG spectrum. This IC has been validated by comparing the measurements of a pre-recorded human ECoG signal with those generated by a model of the signal acquisition chain. This approach, however, does not accurately capture the IC's interface with the body (e.g., 60 Hz noise), which may significantly affect the performance. When tested in an awake monkey, the signals simultaneously measured by this IC and those acquired using a commercial system showed only modest correlations in α (8–12 Hz) and high-γ (70–120 Hz) bands. This can be explained by the dominating effects of flicker and thermal noise at these frequencies. On the other hand, the signals in the β (13–35 Hz) and low-γ (35–70 Hz) bands were only qualitatively compared with no correlation coefficients reported. Recent work [21] reports on an AFE consuming 1.08 μW of power per channel, which is achieved by narrowing the AFE bandwidth and filtering out the noise. A potential problem with this approach may lie in the high sensitivity of the designed $G_m C$ filters to process variation. The proposed AFE has been tested in its ability to reproduce pre-recorded ECoG data and acquire ECoG signals *in vivo* from an anesthetized monkey. However, human testing and direct comparison of recorded signals to those acquired with a commercial-grade system have not been performed. Finally, the work in [22] presents a 64-channel wireless micro ECoG recording system with the front-end achieving a power-efficiency factor (PEF) that is 3× smaller than the state-of-the-art. *In vivo* measurements from an anesthetized rodent show the power increase with respect to the pre-sedation state in δ (1–4 Hz) and θ (4–7 Hz) bands, but very little change in BCI-relevant frequency bands. *Furthermore, none of the above systems were tested in a hospital environment, which is typically characterized by extremely hostile ambient noise and interference conditions.* In summary, while the development of these architectures has been inspired by human BCI applications, their *in vivo* testing in humans and comparison to conventionally acquired ECoG signals are conspicuously missing.

This paper presents the design, experimental validation, and comparative study of two CMOS ultra-low power (ULP) amplifier array and serialization circuitries that constitute core building blocks of two brain signal acquisition (BSA) front-ends. These BSA front-ends can act as the basis for a future, fully implantable ECoG-based BCI system (Fig. 1(a)). The AFE IC will be housed within an enclosure, called the skull unit, to be surgically implanted into the skull [23]. Other building blocks required to develop a complete ECoG-based BCI, e.g., transceiver, power management unit and digital signal processor are intended to be placed in another unit away from the patient's brain. This approach imposes less health hazards for the patient as well as more practical system specifications for a portable, user-friendly solution. All circuits in this work are designed to operate in the weak inversion (WI) region to maximize power efficiency and minimize heat dissipation, while maintaining high gain and low noise operation. *In vivo* human measurements and objective validation against a commercial bioamplifier are done in (1) a human subject using non-invasive EEG cap, and (2) a human subject with subdurally implanted high-density ECoG grid.

The paper is organized as follows. Section II presents the proposed AFE for recording ECoG signals and identifies the criteria and required specifications of the building blocks for designing the system. Sections III and IV discuss the design and implementation of the two BSA front-ends, BSA I and BSA II, respectively. Section V illustrates the electrical and neural measurement results of both front-ends. Finally, Section VI presents concluding remarks and potential extensions of this work.

II. PROPOSED SYSTEM ARCHITECTURE

Responsible for sensing and amplification of microvolt-level brain signals, the amplifier array IC is a critical building block of a BSA front-end. To be employed as a fully implantable device, the signal acquisition front-end should be small in size and consume micro-watt level of power. The system-level diagram of the proposed AFE is shown in Fig. 1(b) [24]. The AFE IC includes fully differential amplifiers, a serializer, and an output buffer all biased in the WI region. The outputs of the array are multiplexed in time to better facilitate input-output



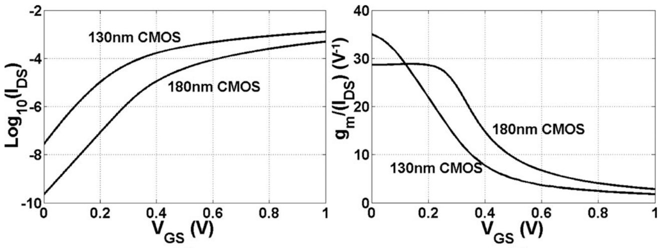
(a) (b)

Fig. 1. Proposed AFE: (a) A cross-sectional view of the envisioned fully implantable BSA circuit, enclosed within a skull unit module. The BSA circuit is connected to a subdurally implanted high-density (HD)-ECoG electrode grid that senses brain signals. (b) Block diagram of the structure showing the brain interface electrodes with their corresponding impedances and BSA comprised of an array of fully differential amplifiers, serializer and buffer.

cable management by reducing the number of wires. The non-overlapping clock generator within the serializer generates N-phase clock signals, each with $1/N$ duty cycle. Non-overlapping clock signals ensure that only one amplifier is connected to the output buffer at a time during the channel switchover. This work presents two ULP BSA front-ends, BSA I and BSA II. BSA I provides symmetrical and complementary signal amplification paths to achieve energy-efficient low noise signal conditioning. BSA II is designed to achieve a high CMRR (i.e., better than 70 dB), thereby reducing the detrimental effect of power-line 60 Hz interference on the recorded signal.

Minimizing both noise and power dissipation imposes stringent design trade-off in an AFE for an implantable system, mandating meticulous considerations at every level of the design process. For example, at the device level, this notion implies that transistors should be designed to operate in a region which yields minimum power consumption for a given IRNoise imposed by minimum detectable ECoG signal power.

It is well-known that the MOS transistors in the WI region achieve maximum $g_m/I_{\rm DS}$-ratio, resulting in the highest power efficiency at the cost of lower operation maximum bandwidth [25], [26]. Fig. 2 demonstrates $g_m/I_{\rm DS}$ and $log_{10}(I_{\rm DS})$ variations with respect to $V_{\rm GS}$ for the two technologies given the same transistor sizes and bias conditions. Referring to Fig. 2(a), a higher subthreshold leakage current and a higher slope are observed in the weak-inversion region for the 130 nm process compared to the 180 nm process. A higher slope corresponds to a larger g_m for the same bias current. This feature translates to a better power efficiency (Fig. 2(b)) and noise performance for transistors designed in this specific 130 nm process. It is noteworthy that the $g_m/I_{\rm DS}$-plot for the 130 nm CMOS process does not show the expected flat region in the deep subthreshold region. This is because BSIM4 device model was adopted for this process by the foundry. On the other hand, the 180 nm process employed PSP device model, which can predict the device behavior in deep subthreshold region more accurately.



(a) (b)

Fig. 2. (a) Drain-source current ($I_{\rm DS}$) vs. gate-source voltage ($V_{\rm GS}$) for the two technologies. (b) $g_m/I_{\rm DS}$ vs. $V_{\rm GS}$ for the two technologies. W/L = 20 μm/2 μm with 10 fingers, $V_{\rm DS} = 1$V for both transistors and body temperature of 37 is considered for simulation.

ECoG signals typically have an amplitude of around 50–100 μV [27], with β and high-γ bands typically providing the most informative features for BCI applications [10]. The IRNoise of the AFE should be kept lower than the noise floor of the ECoG electrodes. Our recorded measurements using a commercial BCI signal acquisition equipment showed that the RMS noise floor, integrated over a frequency range of 8–200 Hz, is typically less than 10 $\mu V_{\rm RMS}$, which is in compliance with the data reported in literature, e.g., [28]. Low noise operation is of particular interest for high-γ band, because the ECoG signal power becomes weaker with frequency [29].

The CMRR and power-supply rejection ratios (PSRR) should be large to attenuate the effect of environmental noise sources (e.g., 60 Hz power-line noise). Assuming an IRNoise level of 2 $\mu\rm V_{RMS}$ in the presence of common-mode interference with 10 $\rm mV_{RMS}$, a nominal 34 dB attenuation (i.e., 74 dB CMRR) is needed so that the output noise and interference voltage magnitudes are equal. In addition, the amplifier should show a high input impedance to lower the effect of common-mode

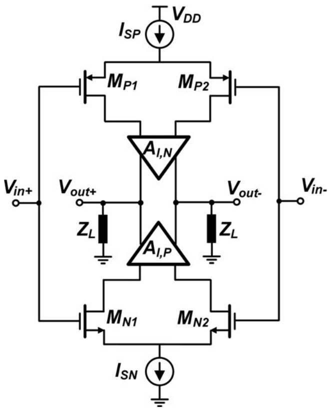
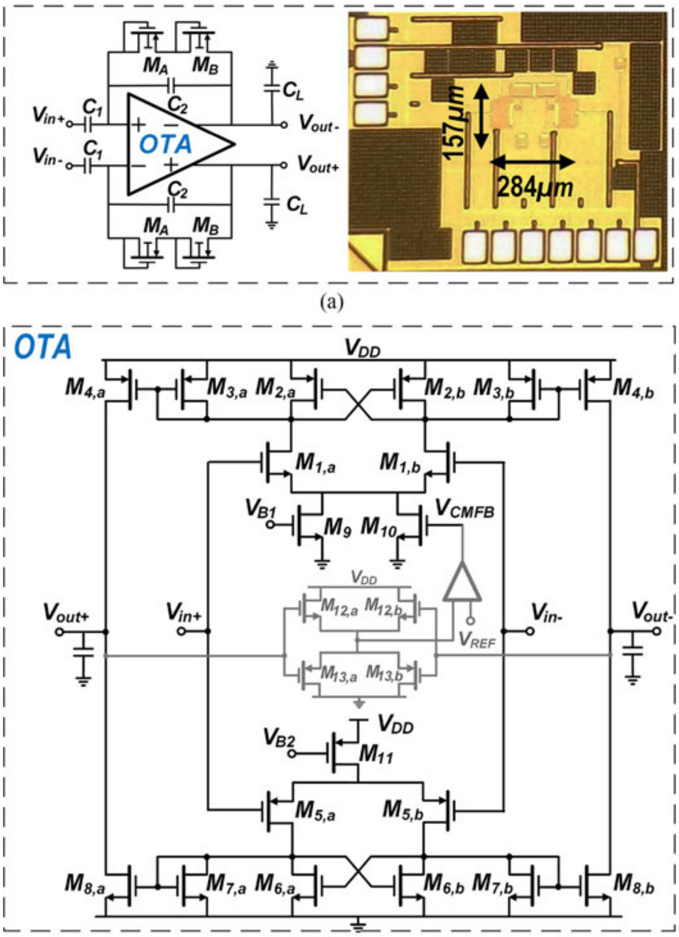


Fig. 3. Complementary input structure of the OTA used in Amplifier I.

interference. This attribute is especially important for multi-channel recordings since the impedance mismatch between electrodes ($Z_{e,1}$, ..., $Z_{e,N}$) as well as the mismatch between the impedance seen from the common reference input (parallel combination of $Z_{in,1}$, ..., $Z_{\mathrm{in},N}$ in Fig. 1) and $Z_{\mathrm{in},k}$ $(1 \leq k \leq N)$ reduces the overall CMRR. Subdural electrodes' impedance have been reported (as well as measured) to be about 1 kΩ [6], thus the input impedance at the frequency of interest should be $\gg$ 1 MΩ [30]. Moreover, large DC offset associated with neural recording electrodes should be eliminated so as to minimize distortion or avoid saturation of the amplifier. Furthermore, electrical shielding and DC isolation are needed between the IC and implanted electrodes. Finally, the crosstalk in a multi-channel system should be mitigated to avoid contamination of the overall information recorded from different channels.

III. BSA I: AN ARRAY OF 64 AMPLIFIER I CIRCUITS AND A SERIALIZER



(a)

(b)

Fig. 4. (a) Amplifier I comprising a closed-loop amplifier with capacitive feedback and its die microphotograph, and (b) the schematic of the complementary NMOS-PMOS OTA [23].

TABLE I
AMPLIFIER I DEVICE SIZES AND OPERATING POINTS

Devices	W/L (μm/μm)	I_D (nA)	g_m/I_D (V^{-1})
M_{1a}-M_{1b}	53.5/1.35	130	34
M_{2a}-M_{2b}	50/10	65	25
M_{3a}-M_{3b}	50/10	65	25
M_{4a}-M_{4b}	3.7/32	1.5	25
M_{5a}-M_{5b}	140/1.2	138	29
M_{6a}-M_{6b}	15/30	69	28
M_{7a}-M_{7b}	15/30	69	28
M_{8a}-M_{8b}	0.4/40	1.5	26
M_9	80/0.36	89	34
M_{10}	80/0.36	170	35
M_{11}	120/0.13	277	25

BSA I incorporates 64 units of Amplifier I and a serializer, as shown in Fig. 1(b). Fig. 3 shows the general block diagram of the OTA used in the Amplifier I, composed of complementary NMOS-PMOS input stage. Intuitively, the signal is amplified by the transconductance gain of the input transistor pairs and subsequently applied to the current gain stage in each of the top and bottom branches ($A_{I,N}$ and $A_{I,P}$). Upon flowing through the load impedance Z_L, the summing current will generate the output voltage. Fig. 4(a) shows the top-level topology of Amplifier I employing an OTA with an RC feedback network. The AC-coupled input provides DC rejection between the recording electrodes and the OTA input, thus providing a layer of electrical safety and isolation between the patient's brain and the amplifier. Fig. 4(b) depicts the transistor-level schematic of the OTA utilized in Amplifier I, including common-mode feedback (CMFB) circuitry (in gray) [23]. The OTA device sizes and aspect-ratios together with operating points of the individual devices are presented in Table I. NMOS and PMOS transistors' body connections are tied to the ground and supply rails, respectively. The minimum headroom for a single transistor biased in the WI region is ~4U$_T$ (where U$_T$ ≈ 26 mV at room temperature) [31]. As a result, the OTA is biased at 0.4 V supply to mitigate large process variations resulting from WI operation, while achieving low power and low noise. The first stage employs a complementary NMOS-PMOS differential configuration with a complementary active load comprising parallel combination of diode-connected transistors and a cross-coupled pair [23], [32]. Cross-coupled pair and diode-connected transistors are identically sized as shown in Table I, thereby having the same transconductance. The effective output resistance of the input stage is thus increased from $\frac{r_{o3}}{1+g_{m3}r_{o3}}||r_{o1}$ (in the absence of cross-coupled pair load) to $r_{o1}||r_{o2}||r_{o3}$, where r_{o1}, r_{o2} and r_{o3} are the drain resistance of M_1, M_2 and M_3, respectively. The active-load devices are sized in a way that no instability or latch-up happens due to the process variation. The size of output transistors M_4 and M_8 are chosen to exhibit large drain resistance and low current consumption at the output stage.

The capacitance ratio C_1/C_2 ($C_1 = 20$ pF and $C_2 = 200$ fF) defines the closed-loop gain with high accuracy so long as the open-loop gain is sufficiently high. High output impedance of the OTA imposes a high impedance load for the feedback and next stage circuits. Pseudo-resistors realized by transistors M_A and M_B (as in [33]) provide large equivalent resistance *R* of few GΩ, self-bias the input stage of the OTA without consuming any additional power for closing the loop, and set the lower 3-dB cut-off frequency ($f_L = (2\pi RC_2)^{-1}$). Compared to pseudo-resistor used in [34], this implementation provides a wider linear range of operation. Assuming all transistors are identically matched (to simplify the analysis), the IRNoise power spectral density (PSD) of the open-loop OTA ($\overline{V^2_{in,OTA}}$) is calculated to be:

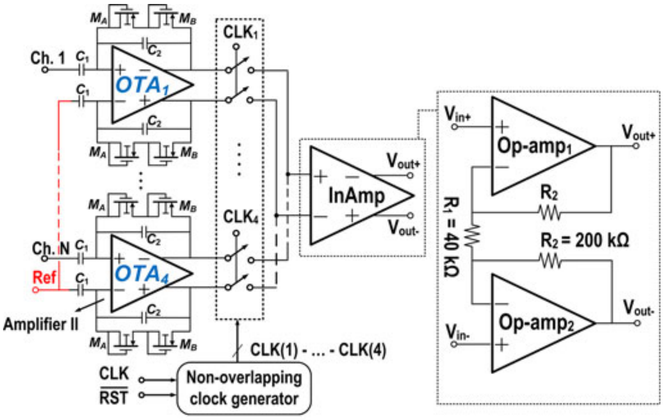
$$\overline{V^2_{\text{in,OTA}}(f)} = \frac{4kT\gamma}{g_{m1}}\left(1+\frac{2g_{m2}}{g_{m1}}\right) + \frac{K_{p,1/f}}{C_{ox}(WL)_1} \times \frac{1}{f}\left[1+2\frac{K_{n,1/f}}{K_{p,1/f}}\frac{(WL)_1}{(WL)_2}\left(\frac{g_{m2}}{g_{m1}}\right)^2\right] \qquad (1)$$

where k is the Boltzmann constant, γ, $K_{p,1/f}$ and $K_{n,1/f}$ are technology-dependent parameters, f is frequency, C_{ox} is the gate oxide capacitor, and *T* is the temperature. γ, the excess thermal noise factor, is slightly lower in the WI region than in the strong inversion (SI) [25]. Note that the complementary structure used in this OTA doubles the overall G_m. Flicker noise and mismatch effects are slightly attenuated by large input transistors and symmetrical circuit layout. In addition, dynamic compensation techniques such as chopper stabilization and autozeroing are commonly used to reduce the effect of amplifier offset and flicker noise [35]–[39]. However, these techniques require switches with low on-resistance to accommodate highly linear operation for autozeroing techniques and low residual input-referred offset voltage for chopping techniques. Thus, a high-swing on-chip clock needs to be generated at the expense of high power consumption. Therefore, we have not used these compensation techniques in the current design. The IRNoise of Amplifier I in Fig. 4(a), $\overline{V^2_{\text{in,tot}}}$, is calculated to be:

$$\overline{V^2_{\text{in,tot}}(f)} = \left(4kTR+\overline{V^2_{\text{in,OTA}}(f)}\right)\left(\frac{f_L}{G_c f}\right)^2 + \overline{V^2_{\text{in,OTA}}(f)}\left(\frac{C_1+C_2+C_{in}}{C_1}\right)^2 \qquad (2)$$

where G_c is the midband closed-loop gain defined by C_1/C_2 and C_{in} is the equivalent input capacitance seen from the input of the OTA.

Sizing of the input transistors is critical due to existing trade-off between $\overline{V^2_{\text{in,OTA}}}$ and $\overline{V^2_{\text{in,tot}}}$. More precisely, large input transistors with low flicker noise will reduce $\overline{V^2_{\text{in,OTA}}}$. On the other hand, a larger device size leads to larger input capacitance, C_{in}, which adversely affects the system sensitivity. Another point to consider is that C_{in} shunts the gate of the input transistor to ground, causing a capacitive voltage division between C_1, C_2 and C_{in}. This, in turn, lowers the differential loop-gain, thereby preventing the closed-loop gain to be accurately defined. Moreover, as f_L decreases, the thermal noise contribution of the pseudo-resistors to $\overline{V^2_{\text{in,tot}}}$ is reduced, while the flicker noise contribution of the OTA to $\overline{V^2_{\text{in,tot}}}$ is increased.



(a) (b)

Fig. 5. BSA II: (a) overall topology, including 4 Amplifier II circuits and one InAmp (b) InAmp implementation.

The serializer in Fig. 1(b) is clocked at 64 kHz and is composed of a custom-designed 6-bit synchronous binary counter, a 6-to-64 decoder and 2 × 64 complementary pass-gate switches for selecting the amplifier channels. A reset signal puts the circuit in an initial state (channel 64) and the clock signal selects the channels sequentially [23].

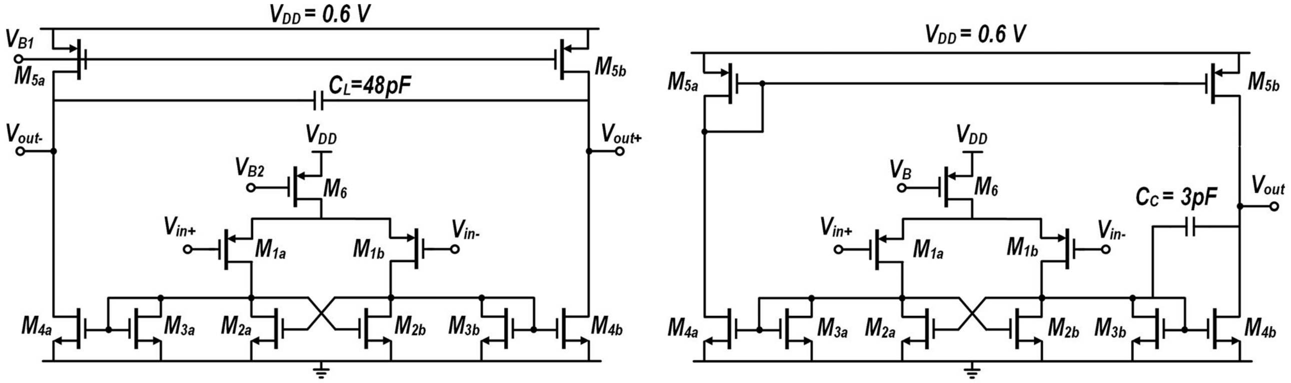
Section V presents the measurement results of the BSA I, which was fabricated in a 130 nm CMOS process [23].

IV. BSA II: AN ARRAY OF 4 AMPLIFIER II CIRCUITS, A SERIALIZER, AND AN INSTRUMENTATION AMPLIFIER

The existence of two signal paths in Amplifier I leads to a degradation in CMRR (≈60 dB). To further elaborate, suppose that the only existing mismatch is the one between each of the input pairs in Fig. 3 (i.e., Δg_{m_N} and Δg_{m_P}). This mismatch directly contributes to the common-mode to differential-mode gain for Amplifier I, which is derived as follows:

$$A_{\text{cm-dm}} \approx \frac{\Delta g_{m_N} \times A_{I_P} Z_{\text{out}}}{(g_{m_{N1}}+g_{m_{N2}})Z_{S_N}} + \frac{\Delta g_{m_P} \times A_{I_N} Z_{\text{out}}}{(g_{m_{P1}}+g_{m_{P2}})Z_{S_P}} \qquad (3)$$

where Z_{out}, Z_{S_N} and Z_{S_P} are output impedances of Amplifier I, I_{S_N} and I_{S_P}, respectively. It is inferred from (3) that the CMRR of Amplifier I can statistically be degraded by a factor of 2 compared to an amplifier with a single path from the input to the output. A high CMRR is important in brain signal amplifiers due to the presence of a strong 60 Hz power-line noise in the amplification band. If not eliminated, major degradation in the output signal-to-noise ratio (SNR) will be seen. To further improve this feature, Fig. 5 introduces the block diagram of BSA II, which is composed of an array of 4 Amplifier II circuits, a serializer, and an instrumentation amplifier (InAmp). Similar to Amplifier I, Amplifier II is realized as a fully differential RC feedback circuit incorporating 200 fF feedback and 18 pF input



(a) (b)

Fig. 6. (a) OTA schematic used in Amplifier II. (b) Op-amp schematic used in InAmp.

AC-coupled capacitors. Matching accuracy of the feedback capacitor limits the achievable CMRR. For instance, it is readily shown that for closed-loop gain of 100 and 10% mismatch of the feedback capacitor, CMRR is lower than 60 dB. The open-loop OTA within Amplifier II employs PMOS input differential-pair with NMOS cross-coupled active loads, as shown in Fig. 6(a). Having one signal path from the input to the output relaxes the mismatch considerations present in complementary signal paths used in the first design.

The IRNoise of the open-loop OTA is calculated to be:

$$\overline{V^2_{\mathrm{in,OTA}}}(f) = \frac{8kT\gamma}{g_{m1}}\left(1+\frac{2g_{m2}}{g_{m1}}\right)+\frac{2K_{p,1/f}}{C_{ox}(WL)_1}\times\frac{1}{f}\left[1+2\frac{K_{n,1/f}}{K_{p,1/f}}\frac{(WL)_1}{(WL)_2}\left(\frac{g_{m2}}{g_{m1}}\right)^2\right] \quad (4)$$

Assuming a single-pole frequency response, it is readily proven that the noise efficiency factor (NEF [40]) reaches a lower-limit of $2\sqrt{n\gamma}$ (where n denotes the subthreshold slope factor [31]) for both OTAs used in Amplifiers I and II if no dynamic compensation techniques are employed. The use of the same closed-loop architecture as in Amplifier I indicates that the IRNoise of Amplifier II is also expressed by (2).

The InAmp, after the serializer, provides further amplification and buffering to the output. It is commonly known that isolated resistive feedback circuitry (R_1 and R_2) provides flexibility in the design of an InAmp and its constituent open-loop op-amps with no concern of loading on preceding circuits [41]. In addition, any variation in R_1 is widely known to only contribute to the differential gain variation and will not increase common-mode to differential-mode gain ($A_{\mathrm{cm-dm}}$) [42], [43]. Therefore, the CMRR is not degraded. As for the contribution of the mismatch between the R_2 resistors ($R_{2\Delta}{=}R_2+\Delta R$) on CMRR, the InAmp's $A_{\mathrm{cm-dm}}$ induced by this mismatch is derived first:

$$A_{\mathrm{cm-dm}} = \frac{E_{\mathrm{CM}}-1}{1+\frac{R_{2\Delta}}{R_1 A_{\mathrm{dm}2}}-\frac{R_{2\Delta}}{A_{\mathrm{dm}1}R_1}E_{\mathrm{CM}}+\frac{1}{A_{\mathrm{dm}2}}} \quad (5)$$

where:

$$E_{\mathrm{CM}} = \frac{1+\frac{1}{A_{\mathrm{dm}2}}\left(1+\frac{R_2+R_{2\Delta}}{R_1}\right)}{1+\frac{1}{A_{\mathrm{dm}1}}\left(1+\frac{R_2+R_{2\Delta}}{R_1}\right)} \quad (6)$$

TABLE II
AMPLIFIER II DEVICE SIZES AND OPERATING POINTS

Devices	W/L (μm/μm)	I_D (nA)	g_m/I_D (V^{-1})
M_{1a}-M_{1b}	152/0.18	510	27
M_{2a}-M_{2b}	12.8/20	255	20.7
M_{3a}-M_{3b}	12.8/20	255	20.7
M_{4a}-M_{4b}	0.8/25	27	16.6
M_{5a}-M_{5b}	16/12	67	22.9
M_6	192/1	1020	27

In deriving (5), the open-loop gains of the op-amps, $A_{\mathrm{dm}1}$ and $A_{\mathrm{dm}2}$, are assumed to be finite, while each op-amp exhibits negligible differential to common-mode gain. The common-mode gain A_{cm} of the InAmp is almost unity. If followed by a high-CMRR amplification stage, the contribution of A_{cm} on CMRR will be negligible. On the other hand, to reduce the impact of $A_{\mathrm{cm-dm}}$ on CMRR, the op-amps need to exhibit large open-loop gain. Large open-loop gain significantly reduces the contribution of R_2 mismatch on the CMRR. Ideally, if the op-amps are perfectly matched ($A_{\mathrm{dm}1}=A_{\mathrm{dm}2}$), $A_{\mathrm{cm-dm}}$ would become zero regardless of ΔR value.

Amplifier II and the InAmp are DC-coupled, eliminating the need for large coupling capacitors. Considering a 39-dB gain for the OTA, the expected differential input amplitude of the InAmp is less than 9 mV, which falls within the input common-mode range of InAmp (0 to $V_{\mathrm{DD}}-2V_{\mathrm{DS,sat}}$ where $V_{\mathrm{DS,sat}}$ is the drain-source saturation voltage).

Fig. 6(a) and (b) show the transistor-level schematics of the OTA used in Amplifier II and the op-amp used in InAmp, respectively. Both amplifiers use similar topology while the devices are sized according to the performance specs needed from each circuit, namely, low noise and high transconductance for the OTA (high driving power and high voltage gain for the op-amp). Tables II and III show device sizes and operating points for the OTA and the op-amp, respectively. All transistors are biased in WI to maximize power efficiency. To achieve a maximum ECoG bandwidth of 200 Hz in the OTA and avoid out-of-band noise accumulation, a large 48 pF capacitor C_L is placed differentially at the output. The input transistors operate in deep WI to maximize their g_m/I_D-ratio so as to reduce the IRNoise

TABLE III
OP-AMP DEVICE SIZES AND OPERATING POINTS

Devices	W/L (μm/μm)	I_D (nA)	g_m/I_D (V^{-1})
M_{1a}–M_{1b}	100/0.18	80	29
M_{2a}–M_{2b}	1/5	40	21
M_{3a}–M_{3b}	1/5	40	21
M_{4a}–M_{4b}	8/5	320	21
M_{5a}–M_{5b}	32/4	320	21
M_6	200/1	160	28

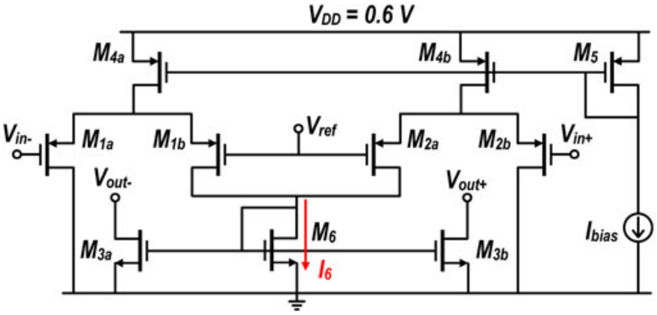


Fig. 7. CMFB circuit used in Amplifier II.

contributions of active-load devices (M_{2a} – M_{2b} and M_{3a} – M_{3b}). PMOS transistors are used in the input differential pair to have a lower flicker noise. Furthermore, the use of a PMOS input pair for the op-amp makes common-mode levels of the OTA output and the op-amp input compatible, thereby making it possible to DC-couple the two. DC-coupling eliminates the need for large decoupling capacitors as well as biasing circuitry of the op-amp inputs. The OTA bandwidth and stability are determined by its output stage where the dominant pole is located. On the other hand, the op-amp's dominant pole is located at its first stage's output node, as its output stage should provide high current drive capability. The op-amp is thus Miller-compensated and its bandwidth is chosen to be $\approx$ 800 Hz in order to accommodate 4 recording channels.

Fig. 7 shows the proposed CMFB circuit to set the output common-mode voltage of the OTA. The drain currents of transistors M_{4a} and M_{4b} are steered to ground or to transistor M_6 depending on common-mode level of V_{in}. M_{3a} and M_{3b} mirror M_6, sinking current from the OTA's output stage, thereby adjusting the OTA common-mode level. Note that the input and the output of the CMFB are physically connected together. The CMFB output currents are expressed as:

$$I_{3a} = I_{3b} = \frac{W_3}{W_6} \times g_{m1,2} \times \left(\frac{V_{in+} + V_{in-}}{2} - V_{\text{ref}}\right) \quad (7)$$

where $g_{m1,2}$ denotes the transconductance of $M_{1a} - M_{1b}$ and $M_{2a} - M_{2b}$, W_3 is channel width of $M_{3a} - M_{3b}$, and W_6 is M_6 width. Input transistors ($M_{1a} - M_{1b}$ and $M_{2a} - M_{2b}$) should remain in saturation region for proper operation of the CMFB. Having few millivolts swing at the OTA's output ensures that no transistor leaves saturation. Transistors M_{3a} and M_{3b} are designed to have long channel length, with negligible loading effect on the OTA. Their parasitic capacitances are absorbed in the OTA's load capacitor. The simulation of the CMFB shows a current consumption of 24 nA and a common-mode phase margin of at least 35°.

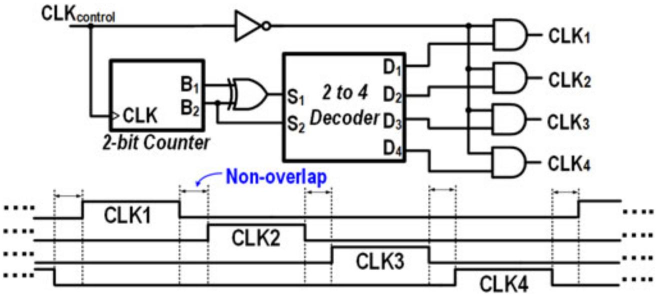


Fig. 8. Non-overlapping clock signals applied to serializer switches.

The circuitry for the serializer logic used in BSA II is presented in Fig. 8. This logic contrives i) non-overlapping clock signals for time-multiplexing, and ii) a gray-coding scheme for a 2-bit binary counter to eliminate race conditions. The serializer clock signal's duty-cycle produces temporal spacing between clocks applied to the serializer switches (Fig. 8). A Gray-code converter is used to convert binary code to Gray code such that the counter exhibits no race condition, which could otherwise result in sparks in the 2-to-4 decoder in Fig. 8. A T-network switch is used for channel selection in this serializer to provide large input-output isolation and minimize the effects of charge-injection and clock-feedthrough.

V. MEASUREMENTS

The functionality of BSAs I and II was verified by electrical and *in vivo* measurements. The EEG test verified the functionality of Amplifiers I and II to detect weak signals in the presence of environmental noise. BSA II was further tested in a hospital environment on a patient who underwent ECoG grid implantation over the motor cortex area. It was experimentally shown that BSA II was capable of recording signals with high output SNR and comparable performance with respect to a commercial EEG acquisition unit, while consuming orders of magnitude less power.

A. Electrical Measurements

Amplifiers I and II were fabricated in 130 nm and 180 nm CMOS processes, occupying 0.044 mm^2 / 0.052 mm^2 die areas, and consuming 0.216 μW / 0.69 μW from 0.4 V / 0.6 V externally provided supply voltages, respectively. Figs. 9 and 10 show die microphotographs of BSA I and BSA II front-end circuits. The first chip (BSA I) occupies 5.45 mm^2, and the second chip (BSA II) occupies 0.352 mm^2 (excluding pad rings). The pad ring incorporates a 2 kV HBM ESD protection circuitry with negligible leakage current. BSA I prototype uses an off-chip buffer to drive commercial signal acquisition unit (MP150 with 12-bit ADC, Biopac Systems Inc., Goleta, CA) [23]. The overall amplification gain for the two AFEs have been measured using Agilent 33250A waveform generator and SMA attenuators, each providing 39 / 58 dB voltage gain and IRNoise

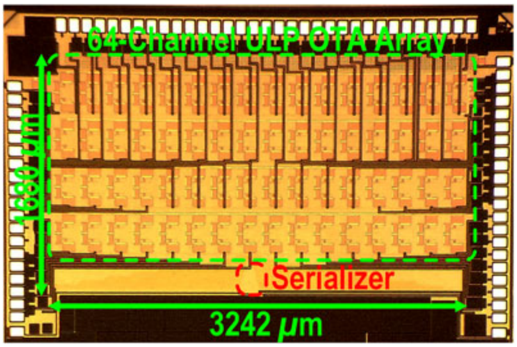


Fig. 9. Die microphotograph of BSA I with 64-channel amplifier array and serializer [23].

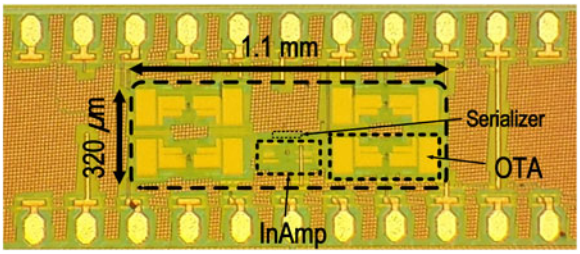


Fig. 10. Die microphotograph of the BSA II with 4-channel amplifier array and serializer.

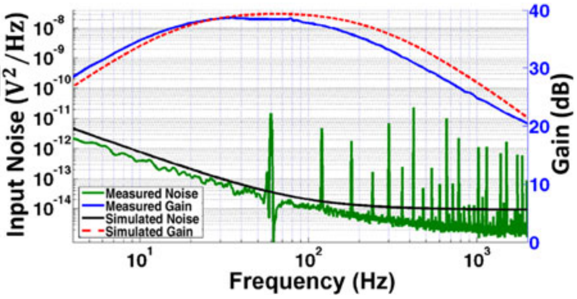


Fig. 11. Measured and simulated Amplifier I gain and noise responses. Note that the sharp peaks were due to 60 Hz harmonics on the unshielded cables [23].

of ~2.19 / 2.3 $\mu V_{\rm RMS}$ across 12–190 Hz / 2–175 Hz of operation bandwidth, respectively (Figs. 11 and 12). Without explicit calibration scheme, the lower-cutoff frequency is not well controlled across process corners. In this work, this frequency was chosen to be smaller than the 8-Hz corner frequency of α-band with negligible effect on noise performance. Simulations show that this lower-cutoff frequency varies from 2 to 10 Hz across process corners.

The 60 Hz interference and its harmonics were removed from the noise plot and calculations in Fig. 12. Linearity and noise measurements were done using Agilent E4448a spectrum analyzer. A low noise off-the-shelf instrumentation amplifier (AD620) was used to boost the noise level and drive the spectrum analyzer. The calculated dynamic range of the Amplifier I at 37 Hz for ~1% Total Harmonic Distortion (THD) was 58 dB. The Amplifier II harmonics for 0.2 mV input voltage at 47 Hz (which is 2 times higher than the expected neural signal amplitude) was lower than the measured noise floor, indicating linear operation. For 150 $\rm mV_{pp}$ signal at 60 Hz, Amplifier I / II exhibits a CMRR greater than 60 dB / 74 dB and a PSRR greater than 58 dB / 70 dB, respectively. Table IV provides the performance summary of the designed amplifiers and comparison with prior art from academia and industry.

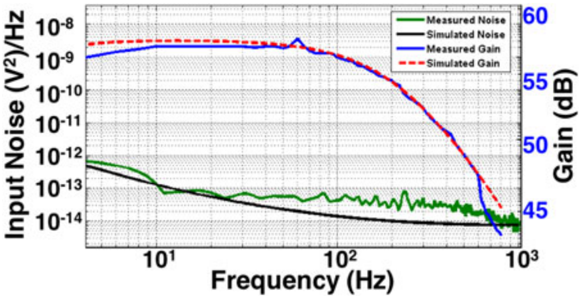


Fig. 12. Measured and simulated gain and noise responses for a single channel of BSA II.

B. Human Neurological Measurements

This study was approved by the Institutional Review Boards of the University of California, Irvine and the Rancho Los Amigos National Rehabilitation Center, and is considered non-significant risk. Three human subjects provided informed consent to participate. The chip was powered by a current-limited (2 mA) supply source. The hospital instruments were disconnected to avoid creation of any unwanted electrical loop. The AC-coupled connection between the electrodes and the amplifiers provides DC isolation.

1) EEG: For two healthy subjects (male, 26 and 27 years old), the impedances of electrodes AFz, Cz, Pz, and Oz in the 10/10 EEG system [44] were reduced to < 3 kΩ using conductive gel. Measurements were performed on one of the subjects using Amplifier I, as follows. EEG from Cz, Pz, and Oz (all referenced to AFz) was recorded at 2353.2 Hz per channel using a data acquisition system (Biopac MP150). This sampling rate corresponds to a sampling period of ~100 μs per channel. The subject was provided verbal cues to alternate between eye opening/closing every 10 s. As a representative example, Fig. 13 shows prominent changes (~10 dB) in the power of the occipital posterior dominant α rhythm at channel Oz in both the time series and the time-frequency spectrogram during this task. This is consistent with classic neurophysiological findings [45].

Measurements were performed on the second subject using Amplifier II, as follows. EEG from channel Oz (referenced to AFz) was split to Amplifier II as well as to a commercial bioamplifier (Biopac EEG100C) and sampled at 50 kHz. The output from both systems was downsampled to 2 kHz and filtered into the 8–35 Hz frequencies in software (see Fig. 14). The two signals exhibited a Pearson correlation coefficient of 0.89, and their envelope powers exhibited a correlation of 0.93. In addition, we recorded multiplexed EEG from electrodes AFz, Cz, Pz, and Oz (all referenced to AFz) using Amplifier II and the results after de-multiplexing in software are shown in Fig. 15.

TABLE IV
COMPARISON AND PERFORMANCE SUMMARY OF AFES

	JSSC 2011 [17]	JETCAS 2011 [19]	TBCAS 2014 [46]	JSSC 2015 [22]	TBCAS 2016 [21]	RHD2000 Intan [47]	Amplifier I	Amplifier II
Power (μW)[†]	2.44	56	23-46	1.4	1.08	7.4[9]	0.216	0.69
Supply (V)	2.8	3.3	+/- 0.6	0.5	1	3.3	0.4	0.6
Gain (dB)	39.4	60	Variable	30	40	45.7	39	39[1]
Bandwidth (Hz)	0.36–1.3 k	300	1–15 k	1–500	0.5–150	0.02–1 k[10]	12–190	2–175
IRNoise (μV_{RMS})[7]	3.07	0.5	13[2]	1.23	N/A[3]	2.4	2.19	2.3
NEF	3.09	4.4	7	3.7	4.52[5]	4.37[9]	4.65	7.22
PEF	26.7[6]	64[6]	58.5[6]	6.9	20.43[5]	63[9]	11.7	31.3
PSRR (dB)	> 80	69	39–93	67	68	75	58	70
CMRR (dB)	> 66	51	51–97	88	82	82	60	74
Area (mm^2)	0.13	86[8]	12.19[8]	0.025	0.085	N/A	0.044	0.052
% THD at mV$_{pp}$ Input	1% (10)	1% (2.6)	1% (4.5)[4]	0.4% (1)	1% (4)	0.8% (10)	1% (5)	<1% (0.2)
Technology	0.6 μm	0.35 μm	0.13 μm	65 nm	65 nm	N/A	0.13 μm	0.18 μm

[†] Power dissipation includes only the front-end amplifier unless otherwise stated. [1] 58 dB for the whole AFE. [2] 7.3 μV_{RMS} for 300–15 kHz. 13 for 1–300 Hz μV_{RMS} [3] 112 nV/$\sqrt{Hz}$ at 150 Hz. [4] Including ADC. [5] Reported for a defined single frequency. Actual value is higher. [6] Value calculated from reported results. [7] Integrated over the bandwidth. [8] Total chip area. [9] Estimated over 1 kHz bandwidth. [10] Bandwidth tunable from 0.02–20 kHz

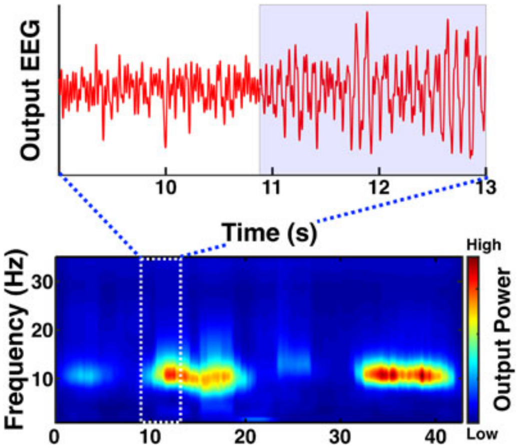


Fig. 13. Amplifier I EEG time series (top) and spectrogram (bottom) from channel Oz with 10 dB increase in the posterior dominant alpha rhythm (8–12 Hz) amplitude when the subject closed his eyes (arrow). The subject closed his eyes at 10 and 32 s and opened again at 20 and 42 s [23].

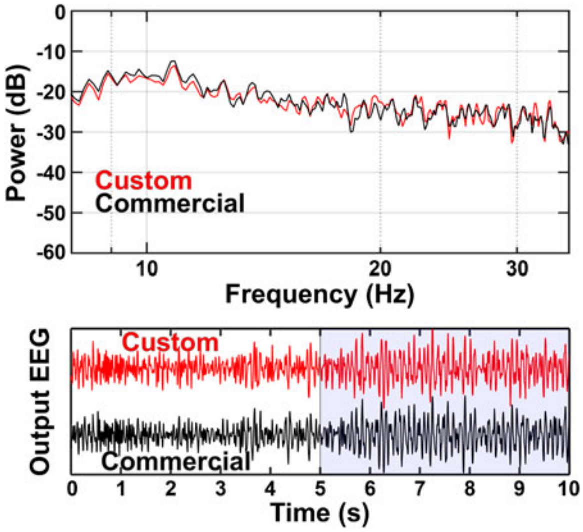


Fig. 14. Top: PSD of the BSA II (red) and commercial (black) bioamplifier from 30 s of EEG data. Bottom: EEG α/β-band (8–35 Hz) time-series data from channel Oz (referenced to AFz) using the BSA II (red) and commercial (black) bioamplifiers. The subject was instructed to alternate between eyes-open (white background) and eyes-closed (blue background).

As physiologically expected, electrodes Oz and Pz exhibit larger amplitudes of the occipital posterior dominant α rhythm during the eyes-closed state.

2) ECoG: One subject (43-year-old male) undergoing ECoG implantation for epilepsy surgery evaluation participated in the study. This subject had an 8×8 grid (Ad-Tech, Racine, WI) of 2 mm-diameter electrodes (4-mm center-center spacing) implanted over the primary motor cortex. Fig. 16 shows the locations of the implanted electrodes (derived by co-registering a CT scan and MRI of the head, as in [48]). The subject completed his epilepsy monitoring procedure and was awaiting ECoG grid removal the next day. Hence, the hospital EEG system was disconnected at the time of measurement. ECoG signals were simultaneously routed to Amplifier II and a commercial EEG100C bioamplifier using unshielded cables, as shown in Fig. 17. Negligible loading effect and source impedance mismatch from EEG100C (2 MΩ input impedance) on Amplifier II is expected due to a relatively small electrodes' impedance (<1 kΩ). ECoG electrodes' impedance is reported to be stable over time [6], eliminating the need for constant monitoring of its value. The output from both amplifiers was recorded at 25 kHz by the MP150 system for 30 s. Note that the subject was asleep during this time and did not participate in any associated behavioral task for further verification of the amplifier array. The resulting signals were then downsampled to 2 kHz in software for further processing. The correlation coefficient between the signals from BSA II and the EEG100C was 0.99 from 8–35 Hz (covering the α and β bands), 0.94 from 35–70 Hz (low-γ band), and 0.72 from 70–120 Hz (high-γ band). Moreover, the correlation between each system's envelope power in α/β, low-γ, and high-γ bands was 0.99, 0.99, and 0.89, respectively. This slight decrement in the high-γ band correlation between the

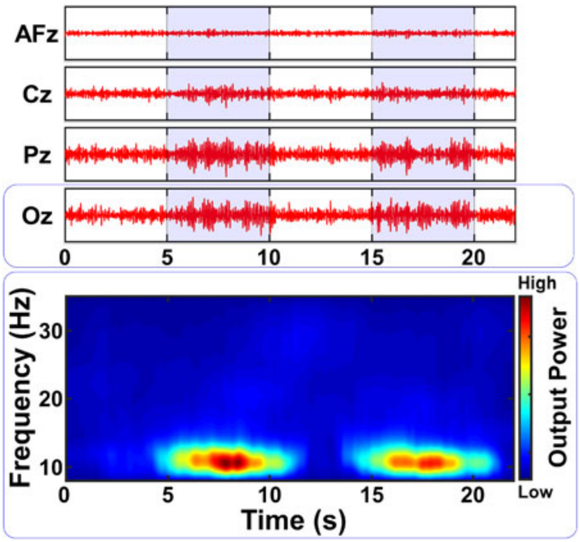


Fig. 15. BSA II EEG α/β-band (8–35 Hz) time-series data (top) and spectrogram (bottom) from channel AFz, Cz, Pz, and Oz (all referenced to AFz) as the subject was instructed to alternate between eyes-open (white background) and eyes-closed (blue background). The channel-multiplexed data from the custom designed IC were demultiplexed in software.

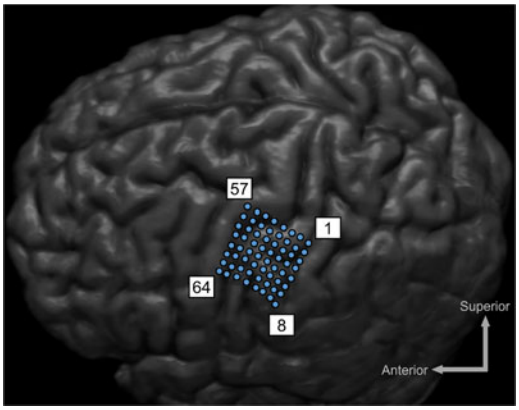


Fig. 16. MRI of the patient with implanted ECoG grid over the left motor cortex. Electrodes 28 and 24 were used as the reference and ground, respectively.

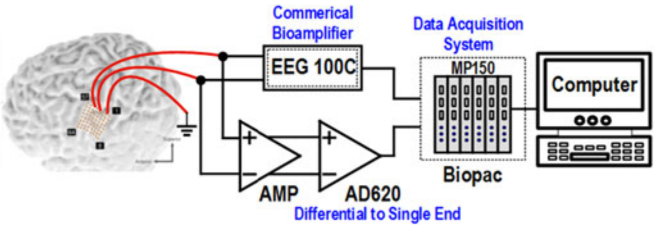


Fig. 17. *In vivo* ECoG measurement setup.

bioamplifiers is expected since the signal power decreases with frequency and approaches the Amplifier II's noise floor. A software notch filter was applied on the signal from 57 to 63 Hz before calculating the correlations. A representative PSD of the recorded signals across the α, β and γ bands (8–120 Hz) and 10-s output time-series of BSA II and its commercial counterpart are shown in Fig. 18, demonstrating qualitative similarities between the two. The peaks at 60 Hz for custom and commercial PSDs are caused by limited CMRR of the signal chain as well as the coupled power line interference to the unshielded interface between the analog output and the external ADC.

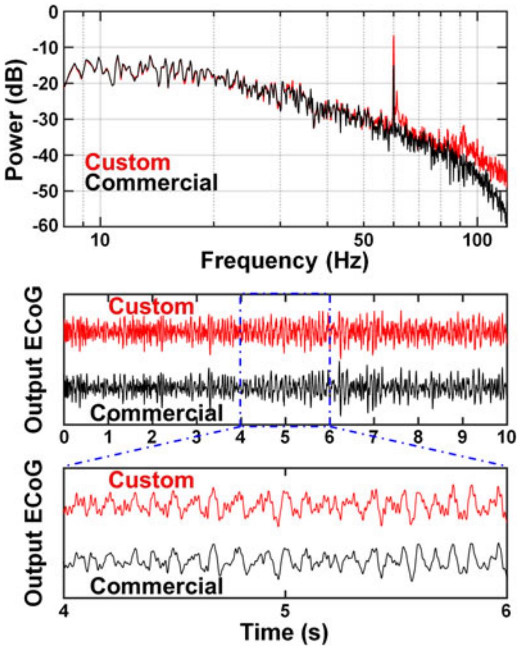


Fig. 18. Top: PSD of the BSA II (red) and commercial (black) bioamplifier from 30 s of ECoG data. Middle: Filtered (8–120 Hz) time-series data from the implanted ECoG grid with the BSa II (red) and commercial (black) bioamplifier. Bottom: Zoomed-in view of the recorded ECoG.

VI. Conclusion and Future Work

Two brain signal acquisition front-ends designed in the WI region were presented. Fabricated in 130 nm and 180 nm CMOS processes, each amplifier within the arrays consumes 0.216 / 0.69 μW, respectively (not including buffer and InAmp). Measured IRNoise across the bandwidth was 2.19 / 2.3 μV_{RMS} corresponding to NEF of 4.65 / 7.22 and PEF of 11.7 / 31.3 [49]. Objective comparison of human *in vivo* EEG and ECoG measurements acquired by our custom IC and a commercial bioamplifier demonstrated that our BSAs were able to record these neural signals reliably. This suggests that the circuit architecture presented in this work can serve as the basis for a highly miniaturized and ultra-low power brain signal acquisition unit for a future fully implantable BCI system. Future work will focus on further reducing the susceptibility of the front-end to environmental noise, e.g., including an on-chip analog-to-digital converter, and incorporating the capability of large interference rejection at low supply voltages in the presence of a sensory feedback stimulation circuitry.

Acknowledgment

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Alireza Karimi-Bidhendi (S'15) received the B.Sc. degree in electrical engineering alongside a minor degree in computer engineering from Sharif University of Technology, Tehran, Iran, in 2013. He is currently working toward the Ph.D. degree in electrical engineering at the University of California, Irvine, CA, USA. In the summer of 2015 and 2016, he was with Indie Semiconductor as an engineering intern, working on low-power oscillators and analog-to-digital converters. His research interest focuses on analog and mixed-signal circuit design for biomedical applications. He received the 2013–2014 Departmental Fellowship and 2014 Henry Samueli Fellowship.

Omid Malekzadeh-Arasteh (S'14) received the B.S. degree in electrical engineering from Northwestern University, Evanston, IL, USA, in 2015. He is currently working toward the Ph.D. degree in electrical engineering at the University of California, Irvine, CA, USA. His research interests include analog and digital circuit design, low-power IC design, and biomedical circuits for brain–computer interface applications.

Mao-Cheng Lee received the B.S. and M.S. degrees from National Chiao Tung University, Hsinchu, Taiwan, in 2011 and 2013, respectively. He is currently working toward the Ph.D. degree in electrical engineering and computer science at the University of California, Irvine, CA, USA. From 2013 to 2015, he was with Airoha Technology Corporation (Mediatek Subsidiary), Taiwan, where he was involved in the design of frequency synthesizers and calibration systems for Wi-Fi, satellite tuner, and Bluetooth products. His research interests include mixed-signal and low-power integrated circuit design.

Colin M. McCrimmon, biography was not available at the time of publication.

Po T. Wang (S'09–M'14) received the B.S. degree in bioengineering from Rice University, Houston, TX, USA, in 2007, and the M.S. and Ph.D. degrees in biomedical engineering from the University of California, Irvine, CA, USA, in 2008 and 2014, respectively.

He is currently a Postdoctoral Scholar with the Department of Biomedical Engineering, University of California, Irvine. His research interests include brain–computer interfaces, embedded systems, and biomedical devices and implants.

Akshay Mahajan received the B.Tech. degree in electronics and communications from the National Institute of Technology, Hamirpur, India, in 2012, and the M.S. degree in electrical engineering from the University of California, Irvine, CA, USA, in 2015. He is currently working in Radio Group in Broadcom Limited, San Diego, CA.

Charles Yu Liu received the B.S.E. degree in chemical engineering from the University of Michigan, Ann Arbor, MI, USA, the Ph.D. degree in chemical/bioengineering from Rice University, Houston, TX, USA, and the M.D. degree from the Yale University School of Medicine, New Haven, CT, USA, and his neurosurgical residency at the University of Southern California affiliated hospitals. He is currently a Professor of neurosurgery, neurology, and biomedical engineering at USC and the Director of the USC Neurorestoration Center. He is also the Surgical Director of the USC Comprehensive Epilepsy Center and the Director of the Neuro-Recovery Programs at Rancho Los Amigos National Rehabilitation Center. His research combines the synergistic aspects of medicine and engineering to develop strategies to restore neurological function in patients with disabilities.

Zoran Nenadic (M'06–SM'12) received the Diploma degree in control engineering from the University of Belgrade, Belgrade, Serbia, in 1995, and the M.S. and D.Sc. degrees in systems science and mathematics, both from Washington University, St. Louis, MO, USA, in 1998 and 2001, respectively. From 2001 to 2005, he was a Postdoctoral Scholar with the Division of Engineering and Applied Science at the California Institute of Technology, Pasadena. Since 2005, he has been with the Department of Biomedical Engineering, University of California, Irvine, where he is currently a Full Professor. His research interests include the area of neuroengineering, biomedical signal processing and pattern recognition, biological neural network modeling, and biomedical devices and sensors. He received the National Science Foundation Faculty Early Career Development Award, the UC Irvine Biomedical Engineering Professor of the Year Award, and the Hiruma/Wagner Award from the Japanese Research Foundation for Opto Science and Technology.

An H. Do received the M.D. degree from the University of California, Riverside/Los Angeles, CA, USA, Thomas Haider Biomedical Sciences Program in 2006. He completed his residency training in neurology in 2010 at the University of California, Irvine, CA, USA. He next undertook fellowship training in spinal cord injury medicine in a joint program at the University of California, Irvine/Long Beach Veterans Affairs Medical Center/Rancho Los Amigos National Rehabilitation Center. He is currently an Assistant Professor in the Department of Neurology, University of California, Irvine. His area of research is in developing and applying brain–computer interfaces to help people with paralysis due to neurological injuries to improve or regain motor function.

Payam Heydari (M'01–SM'09–F'17) received the B.S. and M.S. degrees (Hons.) in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1992 and 1995, respectively, and the Ph.D. degree from the University of Southern California, Los Angeles, CA, USA, in 2001. He is currently a Full Professor of electrical engineering at the University of California, Irvine. His research covers the design of terahertz/millimeter-wave/RF and analog integrated circuits. He is the (co)author of two books, one book chapter, and more than 130 journal and conference papers. He has given Keynote Speech to IEEE GlobalSIP 2013 Symposium on Millimeter Wave Imaging and Communications, served as an Invited Distinguished Speaker to the 2014 IEEE Midwest Symposium on Circuits and Systems, and gave a Tutorial at the 2017 International Solid-State Circuits Conference (ISSCC). He was a Distinguished Lecturer of the IEEE Solid-State Circuits Society from January 2014 till January 2016. He received the 2016–2017 UCIs School of Engineering Mid-Career Excellence in Research Award, the 2014 Distinguished Engineering Educator Award from Orange County Engineering Council, the 2009 Business Plan Competition First Place Prize Award, the Best Concept Paper Award both from Paul Merage School of Business at UC-Irvine, the 2010 Faculty of the Year Award from UC-Irvine's Engineering Student Council, the 2009 School of Engineering Best Faculty Research Award, the 2007 IEEE Circuits and Systems Society Guillemin–Cauer Award, the 2005 IEEE Circuits and Systems Society Darlington Award, the 2005 National Science Foundation CAREER Award, the 2005 Henry Samueli School of Engineering Teaching Excellence Award, the Best Paper Award at the 2000 IEEE International Conference on Computer Design, and the 2001 Technical Excellence Award from the Association of Professors and Scholars of Iranian Heritage. He was recognized as the 2004 Outstanding Faculty in the EECS Department of the University of California, Irvine. His research on novel low-power multipurpose multiantenna RF front-ends received the Low-Power Design Contest Award at the 2008 IEEE International Symposium on Low-Power Electronics and Design. The Office of Technology Alliances at UCI has named him one of ten Outstanding Innovators at the university. He currently serves on the Technical Program Committee of the ISSCC. He served as the Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I, and served on the Technical Program Committees of Compound Semiconductor IC Symposium, Custom Integrated Circuits Conference, and ISLPED. He served on the Technical Program Committees of the International Symposium on Quality Electronic Design, the IEEE Design and Test in Europe, and the International Symposium on Physical Design. He is the Director of the Nanoscale Communication IC Labs.