A 64-Channel Ultra-Low Power Bioelectric Signal Acquisition System for Brain-Computer Interface

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***Abstract*—A 64-channel bioelectric signal acquisition system incorporating a CMOS ultra-low power amplifier array and serializer integrated circuit (IC) is presented. Each amplifier within the array employs a complementary differential topology with cross-coupled-pair active load to achieve ultra-low power and low-noise operation for a nominal gain of 39 dB. The serializer utilizes zero-power complementary switch network which is controlled by an on-chip synchronous counter-based control circuitry. Fabricated in a 130 nm CMOS process with an area of 5.45 mm^2 (excluding pads), the IC is designed to operate in the weak inversion region, resulting in an estimated total power consumption of 14 μW. Each amplifier consumes 216 nW from 0.4 V supply and occupies 0.044 mm^2 of die area. The measured input-referred voltage noise across 190 Hz of amplifier's bandwidth is 2.19 μV_{RMS}, corresponding to a power efficiency factor of 11.7. Experiments show that this system effectively amplifies human electroencephalographic and electromyographic signals.**

***Index Terms*—Electrocorticography (ECoG), brain-computer interface, ultra-low power (ULP), noise efficiency factor (NEF), power efficiency factor (PEF), operational transconductance amplifier (OTA), weak inversion (WI) region.**

I. Introduction

According to the World Health Organization (WHO), up to 500,000 individuals suffer spinal cord injury (SCI) annually worldwide, which can leave those affected with permanent disability [1]. For example, paraplegia (inability to walk) due to SCI substantially decreases quality of life for victims and their family members, and can lead to further complications, such as pressure ulcers and cardiovascular problems. These contribute to a significant economic burden as well as a marked decrease in independence and quality of life. Thus, practical and feasible clinical solutions for restoring motor functions are greatly needed. Brain-computer interfaces (BCIs), which bypass the damaged nervous system and enable intuitive brain-directed control of prostheses, can be one such approach. Non-invasive BCIs have the capacity to restore basic ambulation after SCI [2], [3], although their applicability is limited by the low information content of non-invasively acquired brain signals. Invasive BCIs, on the other hand, have enabled control of a multiple degrees-of-freedom robotic prostheses [4]. However, they utilize bulky, power-hungry general-purpose electronics. Patients are unlikely to widely adopt such BCIs in their current impractical state. Practical BCI systems must, therefore, be highly miniaturized, power efficient, and fully implantable.

This paper presents the design, implementation, and measurement of a 64-channel CMOS ultra-low power (ULP) amplifier array and serializer front-end for a future fully implantable electrocorticogram (ECoG)-based BCI system (Fig. 1(a)). The amplifier array and serializer are designed to operate in the weak inversion (WI) region to maximize power efficiency, while maintaining acceptable gain, low-noise operation and low heat dissipation. Finally, as a preliminary step before testing with ECoG signals, the system was first validated on non-invasive neural signals, including electroencephalogram (EEG) and electromyogram (EMG).

II. System Architecture

The ULP amplifier array and serializer IC is a critical building block for future fully implantable BCI systems, with size and heat/power dissipation as the main constraints. The overall architecture of the proposed front-end is shown in Fig. 1(b). The implantable amplifier array and serializer IC is housed within an enclosure, called the skull unit, and is surgically embedded into the skull. The IC includes 64 fully differential amplifiers and a serializer, all biased in the WI region. The outputs of the array are serialized to facilitate input-output cable management by reducing the number of wires to a total of five, namely $V_{DD}, GND, \overline{RST}, CLK$ and the serialized output.

III. Amplifier Design

A. Amplifier Design Specifications

To minimize power consumption and size, while achieving high quality neural signal acquisition, design specifications were set as follows.

Heat dissipation was optimized by minimizing the DC power of the amplifier array, which constitutes the largest percentage of the overall power dissipation of the skull unit in Fig. 1(a). Operation in the WI region maximizes the transistor's g_m/I_D-ratio, which in turn results in the highest power efficiency [5], [6]. Neural signal properties must also be considered as part of the design specification. Namely, ECoG signals have amplitude in the range of 50–100 μV [7] with β (13–35 Hz) and high-γ (70–160 Hz) bands typically providing the most informative features for BCI algorithms [8]. Hence, a low cut-off frequency at $\sim$15 Hz was chosen to retain these frequency bands, while reducing the flicker noise. The input-referred noise (IRNoise) of the system sets its sensitivity and should be kept lower than the minimum amplitude of the brain signals to be detected. This minimum sensitivity requirement

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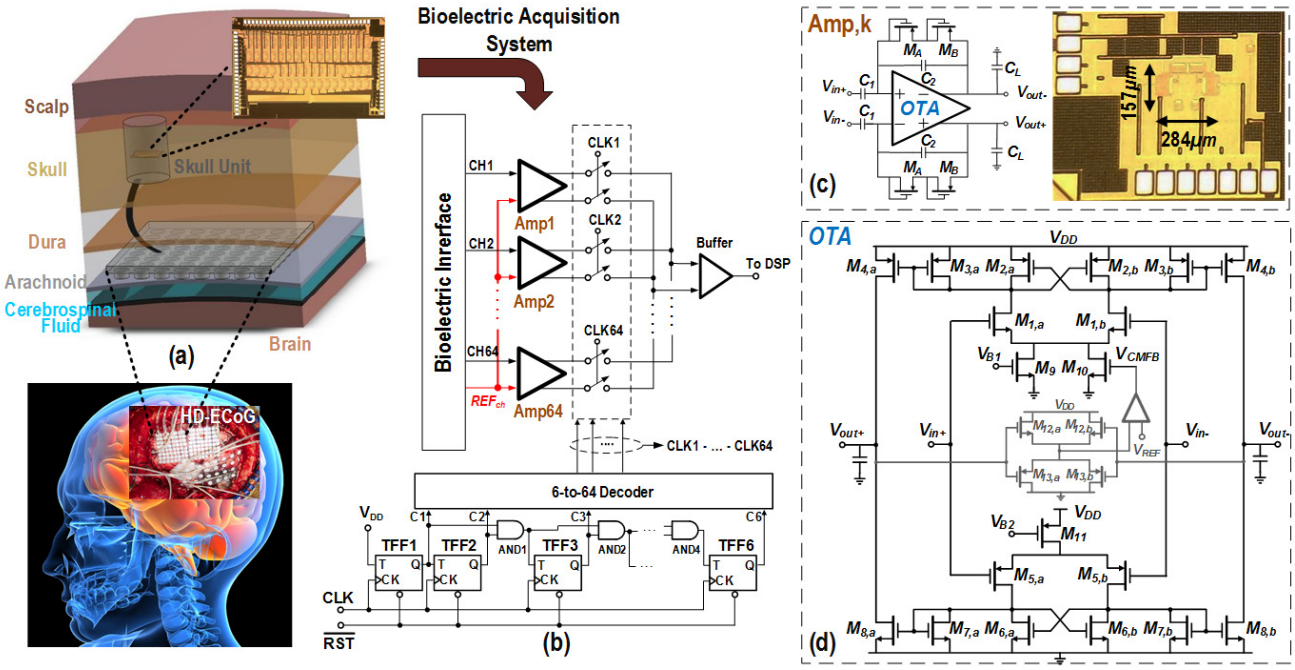

Fig. 1: Overall proposed system: (a) A 3-D cross-sectional view of the envisioned implantable BCI acquisition system, which includes the constituent implantable electronics within an enclosure, acquiring from a subdural 64-channel high density (HD)-ECoG electrode grid. (b) System-level block diagram of the ULP IC, biased in the WI region, comprising an array of 64 fully differential amplifiers and a serializer, which is controlled by an on-chip synchronous counter-based control circuitry. (c) Closed-loop amplifier architecture and die micrograph. (d) Transistor-level schematic of the OTA.

should be met without excessive power dissipation. Lower noise is particularly important since EEG signals (<20 μV [7]) will be used for preliminary design verification. Common-mode and power-supply rejection ratios (CMRR and PSRR, respectively) should be large (e.g., > 50 dB) to lower common-mode noise and mitigate crosstalk in a multi-channel system.

B. Amplifier Circuit Topology

Fig. 1(c) shows the top-level design of the amplifier. This closed-loop amplifier employs an operational transconductance amplifier (OTA) with capacitive feedback. It also isolates the DC path between electrodes and amplifiers, a requirement to operate the amplifier array in the presence of the electrodes' large DC offset as well as for electrical safety. Moreover, the amplifier gain is defined with high accuracy by the capacitor ratio C_1/C_2. The diode-connected transistors M_A and M_B act as pseudo-resistor with equivalent resistance of $R \sim 10^{10}\Omega$ [6], and self-biases the input stage of the OTA without loading its output stage and help set the lower cutoff frequency $(1/RC_2)$. The large effective resistance of pseudo-resistors helps manage sizes of C_1 (20 pF) and C_2 (200 fF) to make a 64 channel device implantable. The lower cutoff frequency is chosen to mitigate flicker noise. Fig. 1(d) depicts the transistor-level schematic of the proposed ULP OTA, including common-mode feedback (CMFB) circuitry (in gray). The minimum headroom for a single transistor biased in the WI region is $\sim 4U_T$ (where $U_T \approx 26$ mV at room temperature) [9]. Biasing the circuit in the deep WI region exacerbates the inherent non-ideal effects of this mode of operation. Therefore, the OTA is biased at V_{DD} of 0.4 V to mitigate those effects, while achieving low power and noise. Large-sized input transistors were used to lower flicker noise and reduce mismatch effects. The first stage employs a complementary NMOS-PMOS differential configuration (M_1, M_5) with an active load comprising a parallel combination of diode-connected transistors and cross-coupled pair. Diode-connected transistors act as a current mirror for the second stage. They also define the common-mode (CM) level of the first stage, eliminating the need for an additional CMFB circuitry. The size of the diode-connected transistors was chosen from the trade-off between their thermal and flicker input-referred noises and the first-stage voltage swing. Cross-coupled pairs help boost the overall transconductance (G_m) by adding negative resistance to the load of input transistor pairs. Note that the complementary structure doubles the overall G_m compared to a regular differential pair, thereby lowering the input-referred noise voltage by a factor of $\sqrt{2}$. Assuming equal device transconductances $g_{m1} = g_{m5}$ and $g_{m4} = g_{m8}$, the simplified OTA input-referred noise is:

$$\overline{V_{in,OTA}^2} = 4kT\gamma/g_{m1} \tag{1}$$

where k is the Boltzmann constant, γ is a constant technology-dependent parameter and T is the temperature. The total gain of the OTA, $A_{V,OTA}$, is given by:

$$A_{V,OTA} = (A_{V_N} + A_{V_P}) \times g_{m4} R_{out} \tag{2}$$

where A_{V_N} and A_{V_P} are the voltage gains of complementary branches of the first stage, and R_{out} is the second-stage output resistance. A_{V_N} and A_{V_P} are designed to provide equal gain to maximize linearity. Sizing of the input transistors is critical due to existing trade-offs between area, gain, input capacitance, input-referred noise of the OTA, and input-referred noise of the closed-loop amplifier, $\overline{V_{in}^2}$, which is expressed as:

$$\overline{V_{in}^2} = \left(\frac{C_1 + C_2 + C_{in}}{C_1}\right)^2 \times \overline{V_{in,OTA}^2} \tag{3}$$

Based on (3), larger input transistors results in an increase in gain and a decrease in $\overline{V_{in,OTA}^2}$. However, larger device sizes also increases OTA input capacitance, C_{in}, which adversely affects the system sensitivity. A CMFB is required for the amplifier to properly define the DC level of the output nodes. Fig. 1(d) also shows the CM voltage detector circuitry, which is based on the work presented in [10]. This detector is followed by a differential to single-ended amplifier to complete the CMFB circuitry. Measurements showed the output DC level linearly tracks the applied reference voltage V_{REF}.

IV. Serializer Design

To serialize 64 channels of ECoG signals, a 64 kHz clock frequency is chosen to satisfy the Nyquist criteria. The serializer should exhibit low-power dissipation; and low channel-charge injection and clock feedthrough to the output, while maintaining high quality signal acquisition. Slightly larger than minimum-sized transistors were chosen for the switch network and its associated control circuitry to mitigate the non-ideal effects in the WI region, such as leakage, process variation, and low noise margin [9].

Designed for a 0.4 V supply, the ULP serializer is composed of a 6-bit synchronous binary counter, a 6-to-64 decoder and 2×64 complementary pass-gate switches for selecting the differential output of amplifiers. The decoder was realized using a combination of four 4-to-16 dual-tree structures. The 6-bit counter utilizes a conventional architecture consisting of six Toggle Flip-Flops (TFF), in cascade. Owing to its low-leakage current in the WI region, a static flip-flop structure was chosen. The signal $\overline{RST}$ resets the circuit in an initial state (channel 64), while channels 1 to 63 are selected by removing reset and applying the respective clock signal.

V. Measurement Results

The amplifier array and serializer IC was fabricated in a 130 nm CMOS process. Fig. 2 shows the die micrograph of the IC with an active chip area of 5.45 mm^2, excluding pad ring. The active die area of the single amplifier is 284 μm × 157 μm (Fig. 1(c)). Consuming 216 nW from 0.4 V supply voltage (i.e., ∼14 μW for the array), it achieves a measured gain of 39 dB across 12 - 190 Hz bandwidth, which closely follows the simulation results (Fig. 3(a)). The measured IRNoise value is ∼2.19 μV_{RMS}, making it possible to measure weak EEG signals. Fig. 3(b) shows the power spectral density (PSD) of the output signal measured with a spectrum analyzer. For a given peak-to-peak input swing varying from 3 mV$_{pp}$ to 5 mV$_{pp}$ (where the output saturates), the measured Total Harmonic Distortion (THD) varies from 0.53% to 0.94%. The calculated dynamic range for nominal ∼1% THD, corresponding to 5 mV$_{pp}$, is greater than 58 dB. The CMRR and PSRR were measured to be greater than 60 dB and 51 dB across the operating bandwidth, respectively. For the present design, an off-chip buffer was used to drive an external acquisition unit (Biopac MP150 with 12-bit ADC).

Table I summarizes the performance of a single amplifier and shows the comparison with relevant prior art. The proposed amplifier achieves Noise Efficiency Factor (NEF) of 4.65 and Power Efficiency Factor (PEF) [5] of 11.7, which is comparable with state-of-the-art designs, yet with an order of magnitude lower power consumption.

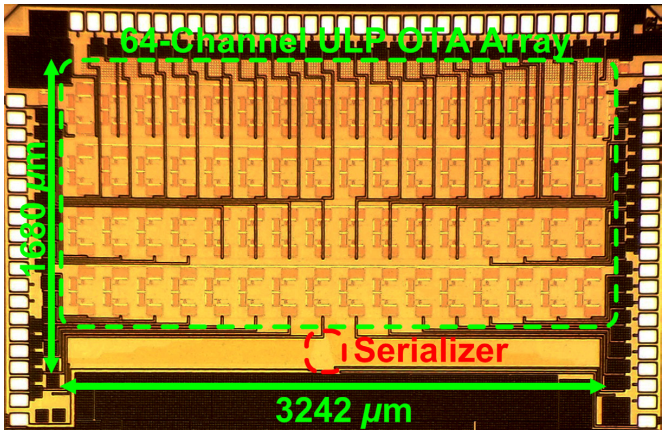

Fig. 2: Die micrograph

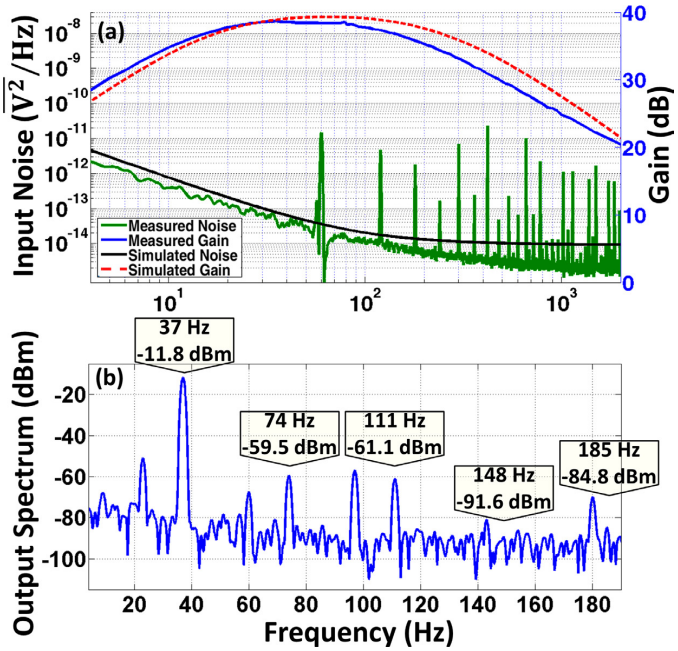

Fig. 3: (a) Measured and simulated amplifier gain and noise responses. Note that the sharp peaks were due to 60 Hz harmonics. (b) Measured harmonic distortion analysis for 3 mV$_{pp}$ input.

To perform electrophysiological validation tests, the IC was wire-bonded on a 100-pin QFN package and soldered to a breakout board. EMG and EEG tests were performed to demonstrate the functionality and system's ability to amplify low-amplitude bioelectric signals. EMG electrodes were placed over the flexor digitorum muscle groups, with the reference immediately distal to the medial epicondyle of a single human subject. EMG signals were recorded at 500 Hz while the subject was asked intermittently to clench and open his hand once every 3-4 seconds (Fig. 4). Based on Fig. 4, both time and frequency domain analyses demonstrated an expected increase in EMG amplitude and broad spectrum power during movement. EEG was sampled at 2353.2 Hz per channel from three electrodes, placed at Cz, Pz, and Oz in the 10/10 EEG system (reference electrode at AFz) on a healthy human subject. The subject alternated between opening and closing his eyes approximately every 10 s. As a representative example, Fig. 5 shows prominent changes (∼10 dB) in the power of the

TABLE I: Comparison and summary of amplifier performance

	[11]	[12]	[13]	This work
Power (μW)	2.08	3.5	1.8	0.216
Supply (V)	2.8	1	1.8	0.4
Gain (dB)	40.9	60	41	39
Bandwidth (Hz)	0.39–295	100	180	12–190
IRNoise (μV_{RMS})	1.66	1.3	0.95	2.19
NEF	3.21	9.38†	4.6	4.65
PEF	28.8†	87†	38†	11.7
PSRR (dB)	75	-	-	>51
CMRR (dB)	66	60	>80	>60
Area (mm^2)	0.16	0.30	1.7	0.044
Dynamic Range (dB) at % THD	63.7 (1%)	-	71† (0.1%)	58 (0.95%)
Technology (μm)	0.5	0.18	0.8	0.13

†Value calculated from reported results.

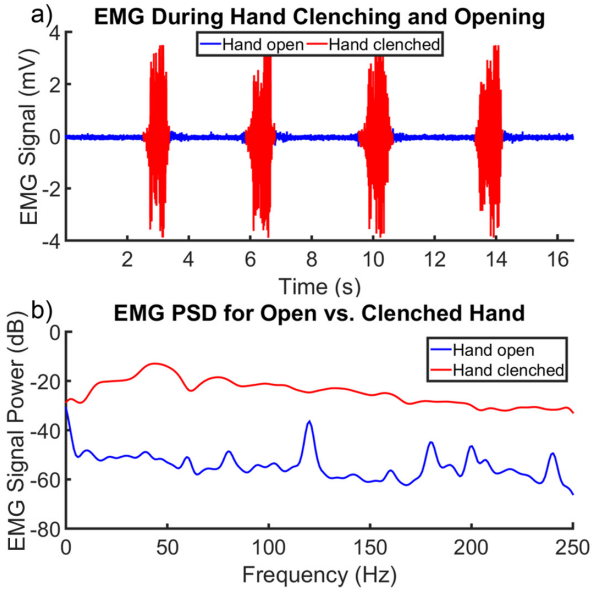

Fig. 4: EMG times series (a) and PSD (b) during hand-clenched (red) and hand-open (blue) states. Note the ∼30 dB broadband increase in amplitude during the hand-clenched state.

posterior dominant alpha rhythm (8-12 Hz) at channel Oz in both the time series and the time-frequency spectrogram when the subject performed this eye opening/closing task. This is consistent with classic neurophysiological findings [14].

VI. Conclusion and Future Work

A 64-channel amplifier array and serializer IC for an implantable brain-computer interface was designed and fabricated in a 130 nm CMOS process. Biased in the WI region, the IC achieved a power efficiency factor of 11.7, an input-referred noise of 2.19 μV_{RMS}, an estimated power consumption of 14 μW, a dynamic range of 58 dB, and a minimum common-mode rejection of 60 dB. Measurements showed that the IC was capable of detecting human EEG and EMG signals, which vary in dynamic range and bandwidth by orders of magnitude. Future work will involve validation of the functionality and performance with invasively acquired ECoG signals.

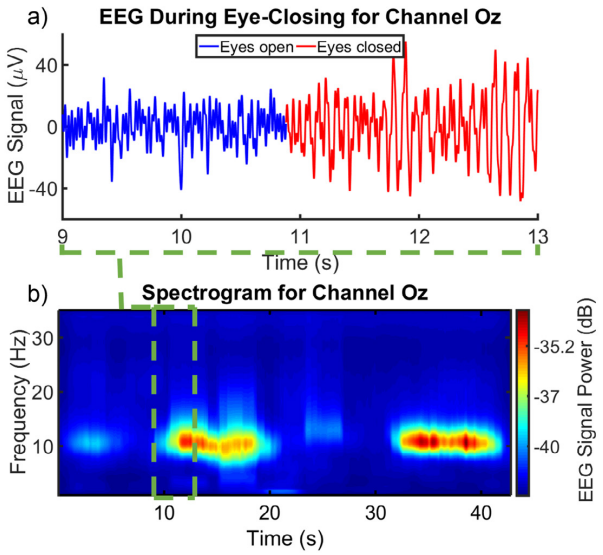

Fig. 5: EEG time series (a) and spectrogram (b) from channel Oz with 10 dB increase in the posterior dominant alpha rhythm (8-12 Hz) amplitude when the subject closed his eyes (arrow). The subject closed his eyes at 10 and 32 s and opened again at 20 and 42 s.

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